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Page overwriting method for performance improvement of NAND flash memories

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Abstract: This paper presents a novel page overwriting scheme for NAND flash memory. It provides significantly improved in-place page update with minimum hardware overhead. It does not require valid page copy for erase operation in order to modify data in a written page. Experimental results show 3.3 ∼ 47.5 times faster page update time with one overwrite allowance and 1.3 ∼ 18.7 with four overwrites allowance compared with conventional method.

Keywords: NAND flash memory, single level cell, multi-level cell, overwrite, write performance

Classification: Storage technology

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1 Introduction

Recently, NAND flash memories (NFMs) are widely used in storage device. Since a NAND flash-based storage device (NFSD) provides greater input/output operations per second and less access latency than a conventional hard disk drive (HDD), NFSD such as a solid state drive (SSD) is gradually replacing HDD. However, NFM has an intrinsic limitation referred to as *erase-before-write* [1]. Erase-before-write requires that a data block containing pre-written pages must be erased before new data is written to that block because NFM does not support page overwrite. Typical page data update is achieved by copying valid pages, erasing the block, and writing new data. And it becomes a significant system performance bottleneck.

Previous works avoid copying valid pages and erasing the block upon a page update is to utilize log blocks [2, 3]. When a page update is needed, this method redirects new data to an empty page in the log blocks, instead of erasing the original block. However, there is only a small number of log blocks to handle overwrite cases and when the log blocks are fully occupied, a victim log block should be selected and erased for new overwrites. To create a new log block, NFM needs to copy valid pages from a used log block and erase it. And it significantly reduces the overall write performance of NFSD. For example, if a log block contains many valid pages and that block needs to be erased, the write performance is degraded due to the time for copying valid pages and erasing a block [4].

In this paper, we propose a page overwriting scheme which does not require an erasing operation for a dedicated block. To avoid erase-before-write, we utilize multi-level-cell (MLC) technology. While previous works on MLC technology focus on space efficiency [5, 6], this scheme focuses on implementing overwrite capability to improve the write throughput. The only additional hardware is four flag bits per page to store the information on the number of overwrites and counting circuitry as shown in Fig. 1. The proposed scheme is implemented in NFM with early 20 nm tech node.

2 Proposed page overwriting scheme

A flash memory cell consists of an n-channel MOSFET with a floating gate (FG) storing electrons and its bit value is determined by the amount of charge trapped in the FG. A write operation (*i.e.* program operation) is to accumulate negative charges in the FG, resulting in state "0", while an erase operation removes negative charges from the FG, resulting in state "1".

There are two cell types for flash memory devices: single-level-cell (SLC) and MLC. SLC devices store one bit of information per cell and MLC devices store multiple bits of information per cell. While SLC requires only two states to store a bit, MLC requires multiple states on a voltage window to store multiple bits, as shown in Fig. 2 (a). To implement the page overwrite without an erase operation, we utilize the multiple states of MLC.

Fig. 2 shows the behavior of cell states as we overwrite multiple times when the maximum number of overwrites (MNO) is set to 2. Initially, all

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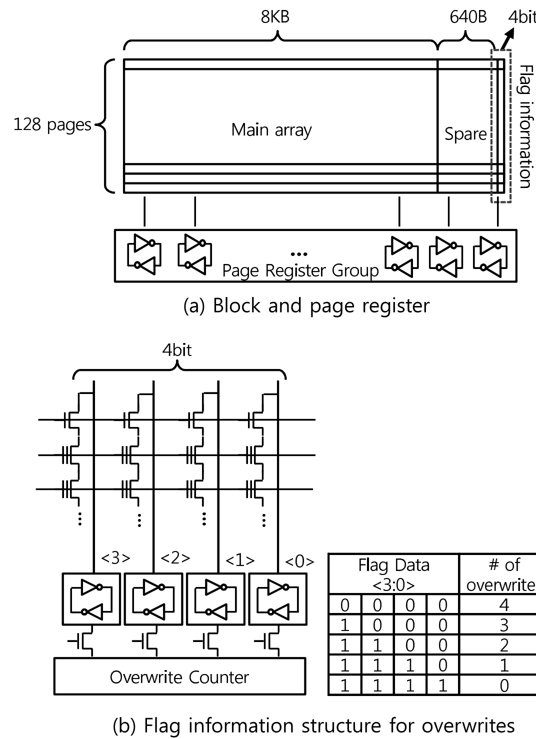

Fig. 1. NFM block structure for page overwrite

cells in a page are in the erased cell state "1" indicated by ① in Fig. 2 (b). When a page is written for the first time, the page data consists of state "1" and "0". Cells in state "1" stay at the initially erased state while cells in state "0" move up to a new voltage state, which is indicated by ② in Fig. 2 (b). When the page needs to be overwritten, the overwrite is executed in two steps. In the first step, all cells in state "1" on that page move up to the voltage state "0" of the initial write indicated by ③ in Fig. 2 (c). We call this a "pseudo erased cell state", which represents a new erased cell state "1". At the same time, state "0" is written into the least significant bit (LSB) of flag data as shown in Fig. 1 (b) to indicate that a page is overwritten once. In the second step, cells with the LSB flag becoming the state "1" after the first overwrite stay at the pseudo erased cell state while cells becoming the state "0" after the first overwrite move up to a new voltage state, which is indicated by ④ in Fig. 2 (c). This two-step procedure is repeated again if the second overwrite occurs, resulting in new two voltage states as shown in Fig. 2 (d). Assuming that the size of the voltage window is restricted by flash memory technology, the maximum number of overwrites is determined by the width of voltage distributions and read margins - the distance between two neighboring voltage distributions.

To read the overwritten pages, a read operation is modified. As shown in Fig. 2 (b), if the cell is located in the voltage state lower than the read voltage (RV_0), the output value of data is "1". When the page is overwritten, the read voltage must be increased according to the number of overwrites as shown in Fig. 2 (c) and Fig. 2 (d). To expedite the read process, a required read voltage refers to four flag bits within the same page as shown in Fig. 1 (b).

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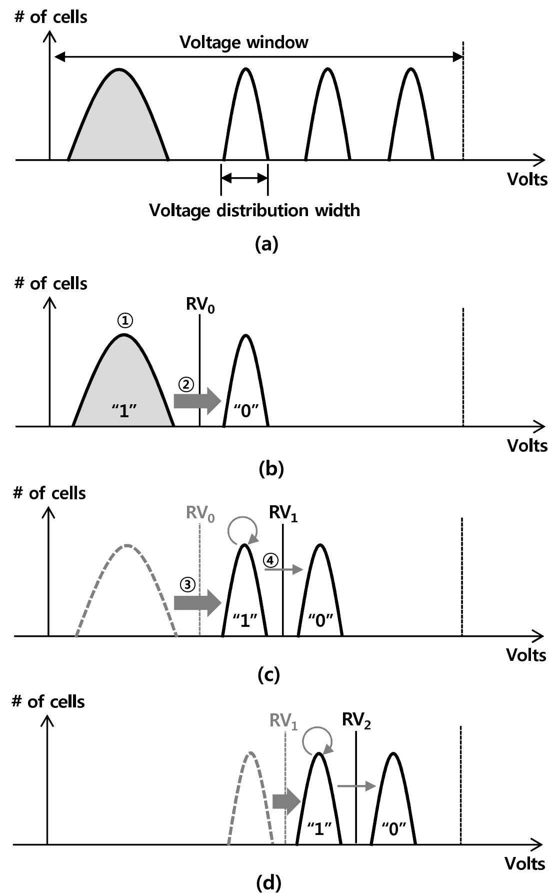

Fig. 2. Cell states after overwrites for MNO set to 2

Thanks to these information, the read operation for the overwritten page is performed in two steps. The first step is to read with the reference level RV_0. This determines whether the page is overwritten or not. If the page is not overwritten, *i.e.* flag bits are 1111, the read operation is completed and the page can output the data. Otherwise, the read voltage is set to a proper level, *e.g.* RV_1 or RV_2, based on the number of overwrites stored in flag bits. This modified read operation leads to the reduction in the read throughput. However, this degradation does not become a major issue because the overall system performance is dominated by the write throughput and our proposed scheme improves the write throughput significantly.

Another issue is the reliability features. The block endurance is degraded due to the smaller margin between two neighboring voltage states for the higher MNO. However, if the block endurance of proposed scheme is more than conventional MLC features, this scheme is able to prolong the block life time.

3 Experimental results

In order to evaluate the proposed scheme, we measure the write time of NFM fabricated with early 20 nm technology node. Fig. 3 (a) shows the write, erase, and update time of the conventional NFM (left side), which are normalized to the write time for SLC-type cells, and the normalized

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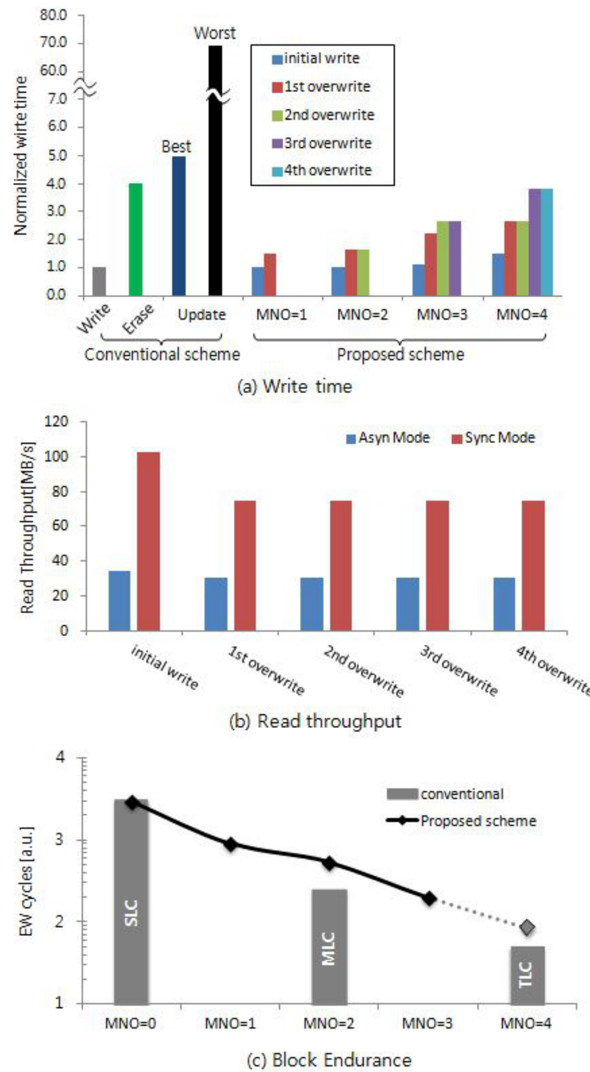

Fig. 3. Write, read performance and block endurance

write time of the proposed scheme for four different MNO values (right side). The best update time represents the case where only one valid page copy occurs whereas the worst time represents 63 valid page copies. When we allow one overwrite (MNO=1), the worst case overwrite time is 3.3 to 47.5 times less than the page update time of conventional NFM. For MNO of 4, the reduction is a factor of 1.3 to 18.7. When we compare the initial write time for four MNO values, it increases from 1 to 1.5 times as MNO increases. This results from the following facts: the number of cell states within the voltage window increases from three (MNO=1) to six (MNO=4) and supporting more states decreases the width of voltage distribution per state given a fixed voltage window size. And it takes longer time to write the state having the narrow width for voltage distribution. For the same reason, the first overwrite time for four different MNO values increase as the MNO number increases. Significant reduction in update (or write) time of the proposed scheme leads to huge improvement in write throughput.

Fig. 3 (b) shows the read performance in terms of throughput. The equa-

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tion for read throughput is shown in (1) [4]

$$Throughput(read) = \frac{Page\ size}{Read\ time + Data\ output\ time} \quad (1)$$

where *Page size* is 8 KB plus 640 B (spare area). *Read time* represents the time required for transferring cell data to the page register. *Read time* for the overwrite scheme increases by 1.8 times due to an additional read. *Data output time* is the time used to read out one page from the page register. Our test device supports both asynchronous and synchronous DDR interface up to 200 MB/s. Therefore, read throughput is degraded by roughly 10% for asynchronous mode and 27% for synchronous mode as shown in Fig. 3 (b). However, overall system performance is significantly improved because the total throughput is dominated by the write performance.

Fig. 3 (c) shows the block endurance between the proposed scheme for MNO values and conventional NAND flash for SLC, MLC and triple level cell (TLC). In the experiments, we supposed that error correction code (ECC) can handle 40 bit errors per a partial page 1 KB. The block endurance is degraded for the higher MNO. When we compare MNO=0 for MNO=3, Erase/write (EW) cycles decrease by 1/15. In case of MNO=4 and TLC, the value of the block endurance was extrapolated because we failed to extract data. However, the proposed scheme exceeds block endurance features compared with conventional NAND feature.

4 Conclusion

We propose a novel page overwriting scheme for NFM. This scheme provides in-place data update upon a page update without an erase operation until the overwrite number of a block reaches MNO. The proposed scheme is implemented with early 20 nm tech node. The results show that the proposed scheme improves the page update time by up to a factor of 47.5. We envision that our proposed scheme can configure part of NFM as an overwritable flash memory region which accommodates frequently updated data. We are currently developing a novel flash translation layer (FTL) for the proposed scheme.

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